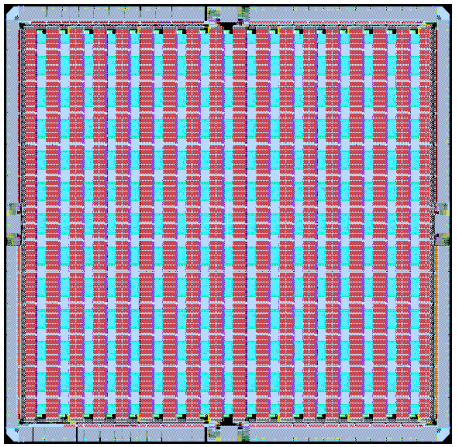
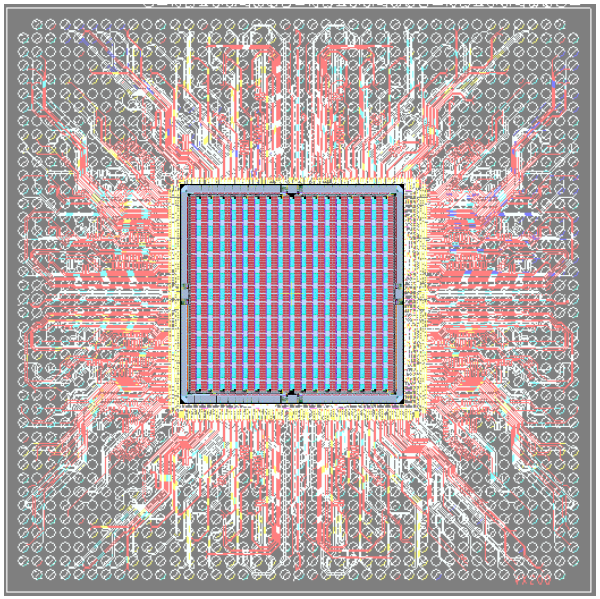
A 180 GFLOP/s, 15 GFLOP/W, 500 million transistor FPGA in 90nm CMOS

Functional Vx200 FPGA silicon



- TSMC 90nm process; Large die with 500M transistors
- Highest monolithic compute power: 180 Single Precision GFLOPs
- Memory Bandwidth: 40GB/s external, >1TB/s internal
- Silicon proven with ATE and in lab

Velogix FPGA FPU Family - Preliminary Data Sheet	
Velogix FPGA	**VX200**
Logic and Routing Cells	41440
Equivalent Logic Cells	49728
Total Flip-Flops	82880
VxSPE - Velogix Signal Processing Elements	204
32x24 2-port Register Files	816
24K Dual Port Block Mem	408
Total RAM MegaBits	10.42
PLLs	24
User IOs	830



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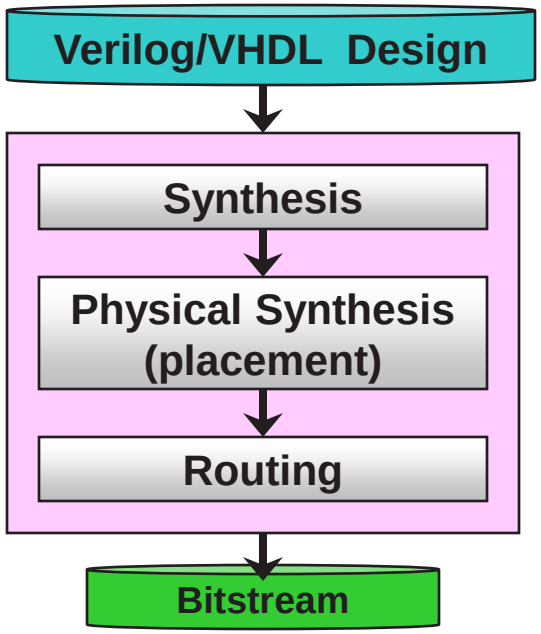
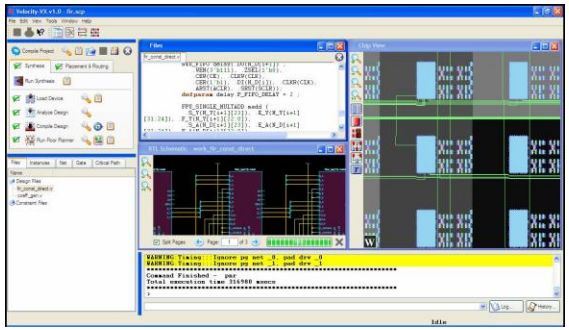
Velocity VX RTL Design Software Solution





- **Complete RTL-to-bitstream software solution**
  - Integrated Physical Synthesis and routing provides 5x faster timing convergence
  - Multi-million gate designs routed
  - User-friendly push-button design flow with industry standard constraints
  - Tested on >100 design regression suite
  - Inference and instantiation of hard macro units including floating point units
  - Zero “failed to route” designs
- **Minimal switching cost**
  - Accepts existing FPGA designs

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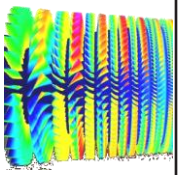
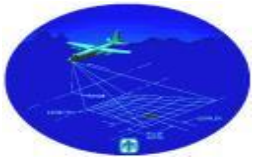
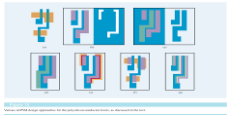
Real Problems, Real Solutions, Real Value

Market Segment	Key Problems	Current situation	Break-through goal	Breakthrough requirement
HPC  	CFD simulation too slow- $1B/yr turbine blade maintenance	Simulate one fan blade in 46 hours	Simulate full turbine in minutes- save $100M/yr	>100 Single Precision GFLOPS
	Black-Scholes evaluation	5K trades/sec	50K+ trades/sec	>100 Single Precision GFLOPS
Imaging  	View internal organs during surgery	Snapshots every few seconds	Real time video of internal organs	200 Single Precision GFLOPS
	SAR to see through fog, clouds & foliage	Snapshots every few seconds	Real time video rate imagery	100 Single Precision GFLOPS
Industrial  	RET simulation	Low accuracy simulation in hours	Full simulation in minutes	100 Single Precision GFLOPS
	Wafer Inspection	Inspection interrupts processing	Real time Inspection	160 Fixed-point GOPS

100-200 GFLOPs is the disruptive performance barrier

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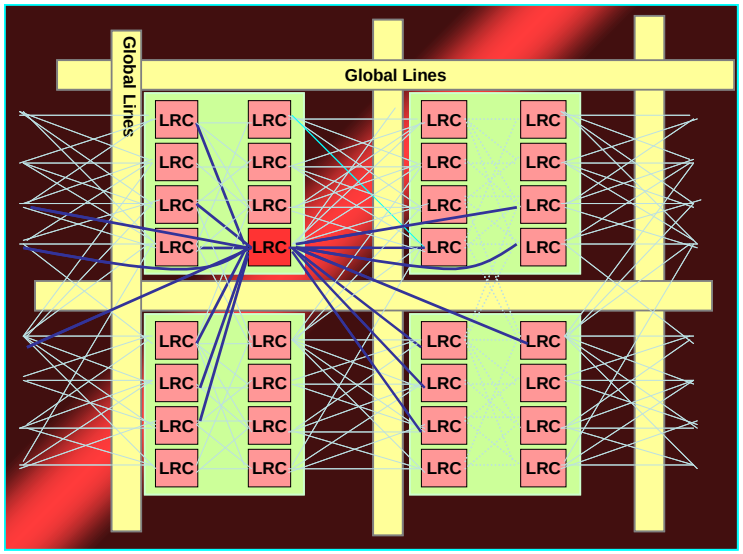
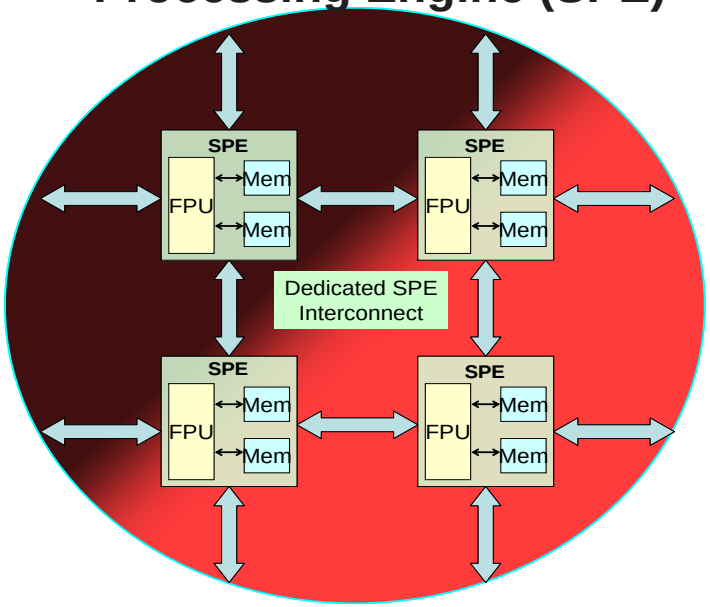
Velogix Programmable Logic Architecture – Powerful Fabric + Market Optimized engines

Next generation programmable logic fabric



- Push-button timing driven routability for full chip multi-million gate designs
- Interconnect architecture tuned for higher clock frequencies
- Offers 2x performance for select data path intensive designs

Embedded Signal Processing Engine (SPE)



- Processing Units integrate compute (FPU/MAC) and storage (memory, register file) blocks
- Two-dimensional bus-based interconnect between integrated processing engines offer predictable performance of 450 MHz
- 17x12 (204) engines in Vx200 offer 180 Single Precision GFLOPs

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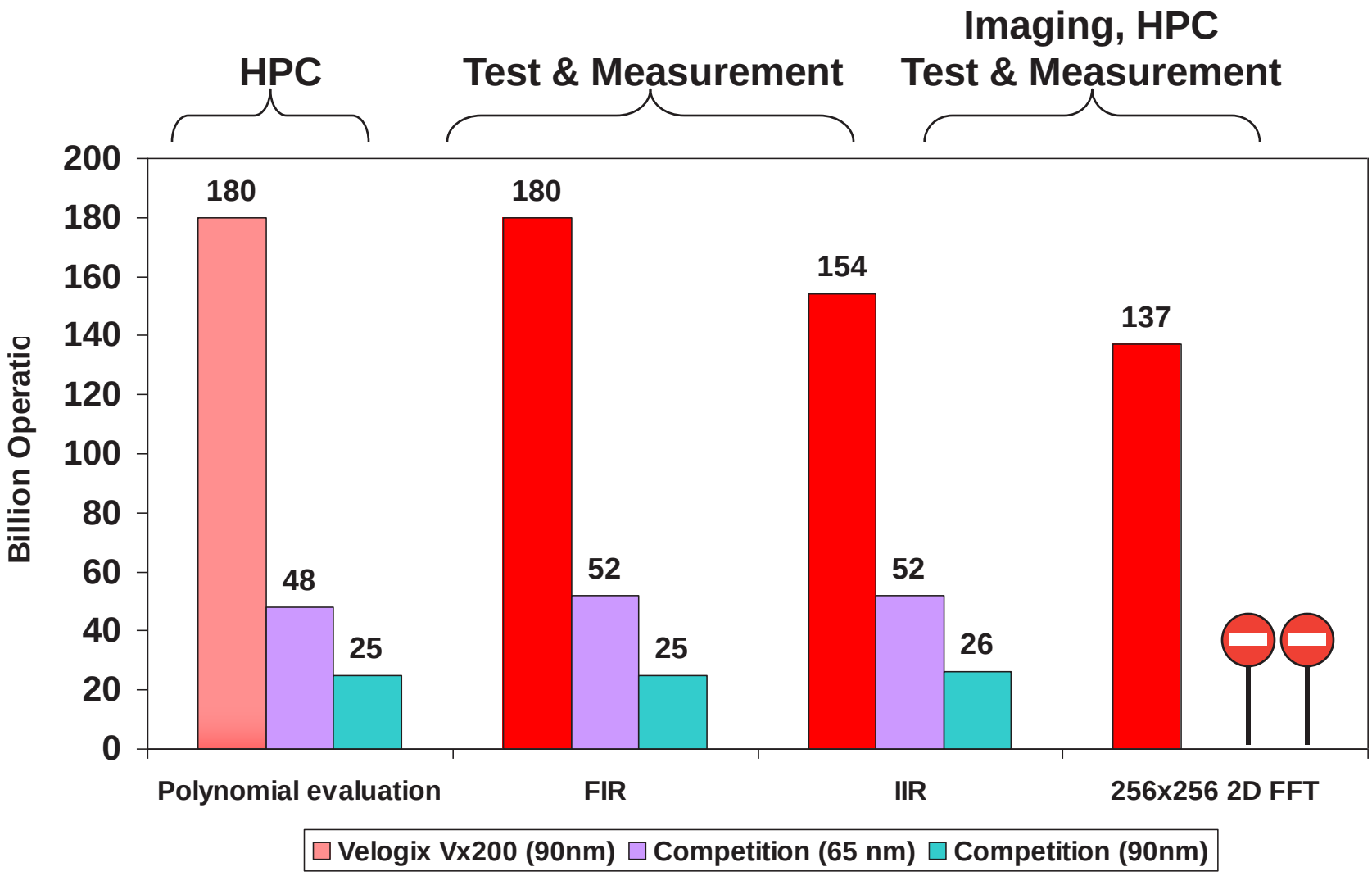
GFLOP Performance Comparison



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Full Chip Design Performance

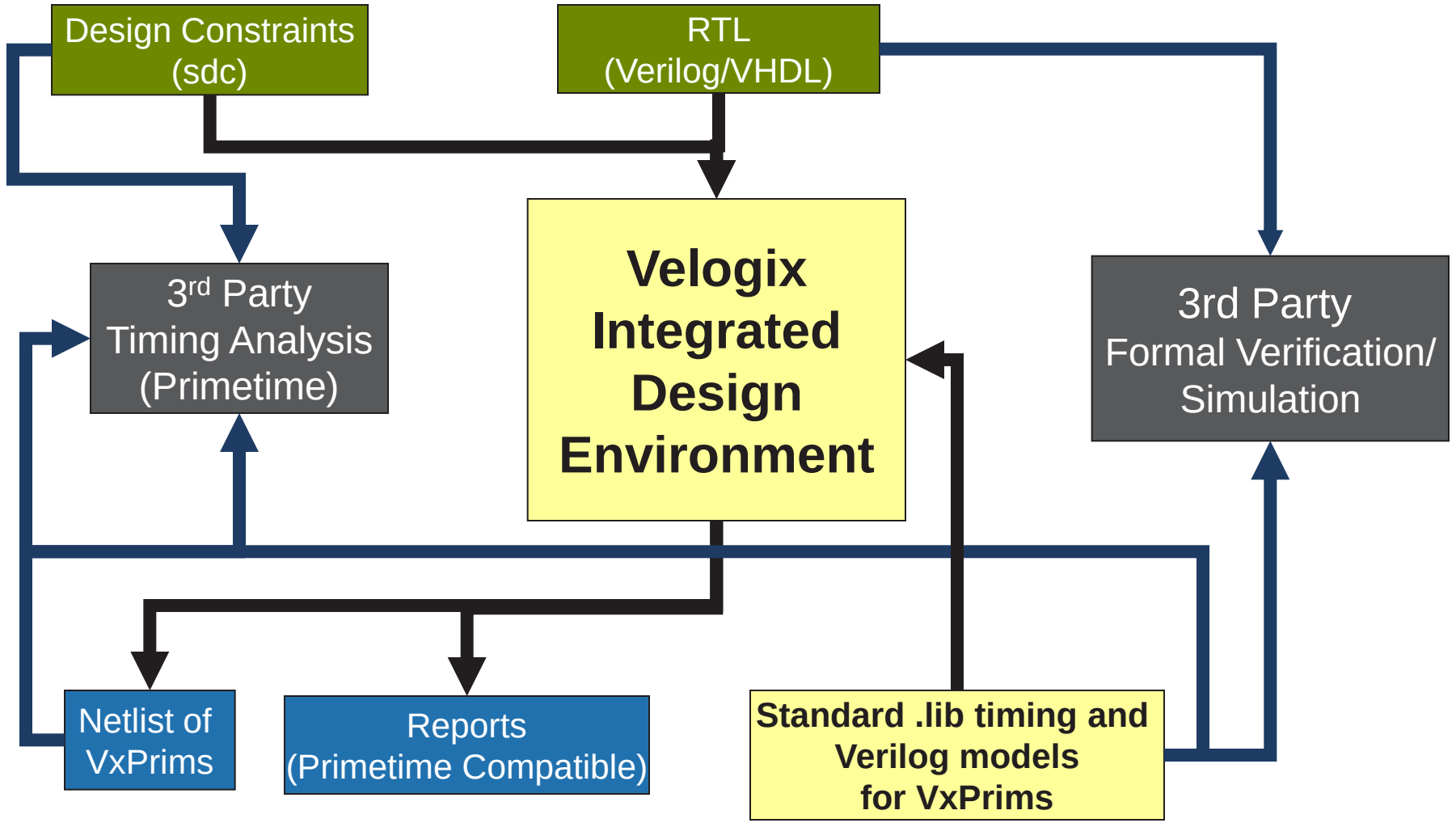
	Type	Performance	Logic Cells Used	Logic Utilization	Compute Units Used	Compute Unit Utilization	
FIR	Floating	180 GFLOPs	12,740	26%	200	98%	
IIR	Floating	154 GFLOPs	7,350	15%	175	86%	
Polynomial Evaluation	Floating	180 GFLOPs	16,170	33%	200	98%	
256x256-2D FFT	Floating	137 GFLOPs	7,350	15%	175	86%	
SSG	8-bit Fixed	400 GOPs	40,670	83%	800	98%	

High Performance maintained even with high utilization

Power Efficiency Comparison (1-D FFT)

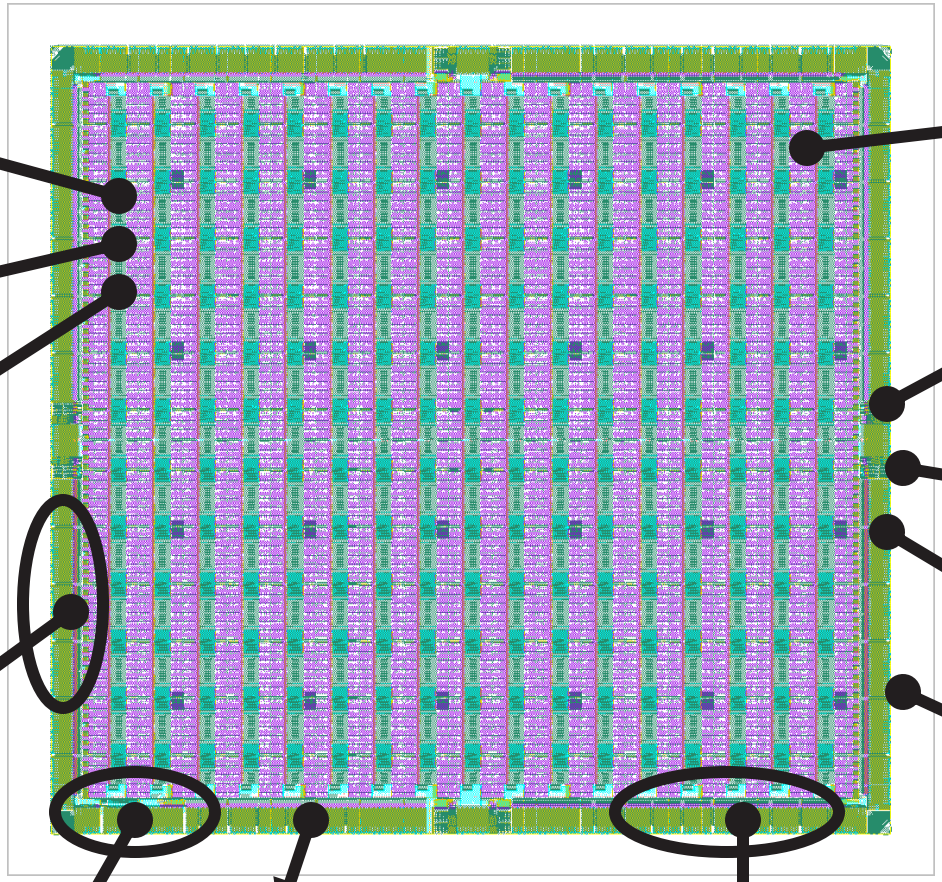
	Performance (SP GFLOPS)	Power dissipation (W)	Power efficiency (SP GFLOP/W)
Vx200	120	8	15
Quad core x86	22	105	0.21
GPUs	52	100	0.52
Xilinx LX 220	40	15	2.7
Cell	91	100	0.91

Standardized timing and verification flow



Standardized SDC based timing and model based verification flow

Vx200 Chip Architecture



DSP Hardware
•Floating Point MADD
•Fixed Point MAC

Dual Port
Block RAM

2-port
Register File

Single Ended
IO Subsystem

Dedicated
IO Bank

High Speed
Configurable
LVDS
IO Buffer

LVDS
IO Subsystem

Programmable
FPGA fabric

PLL

Output Clock
Synthesizer

High Speed
Configurable
Single Ended
IO Buffer

DLL

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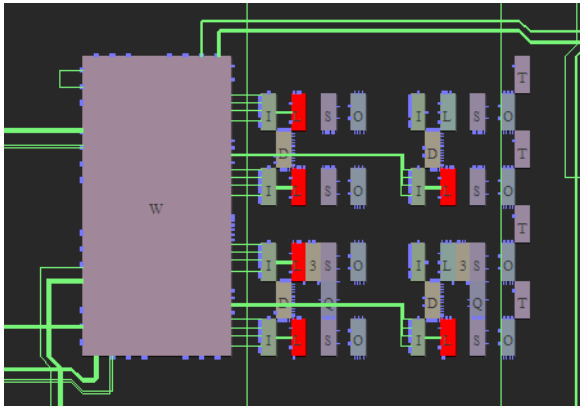
Next Generation Programmable Logic Fabric



Optimized for push-button routability and more performance for the same area

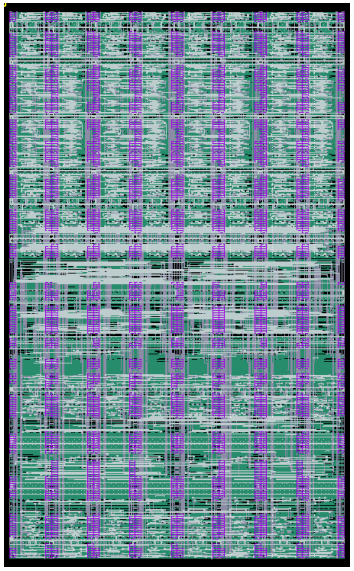
Optimized local connections for critical path delays

Seamless integration of hard macro blocks

Symmetric fabric connection across hard macro blocks

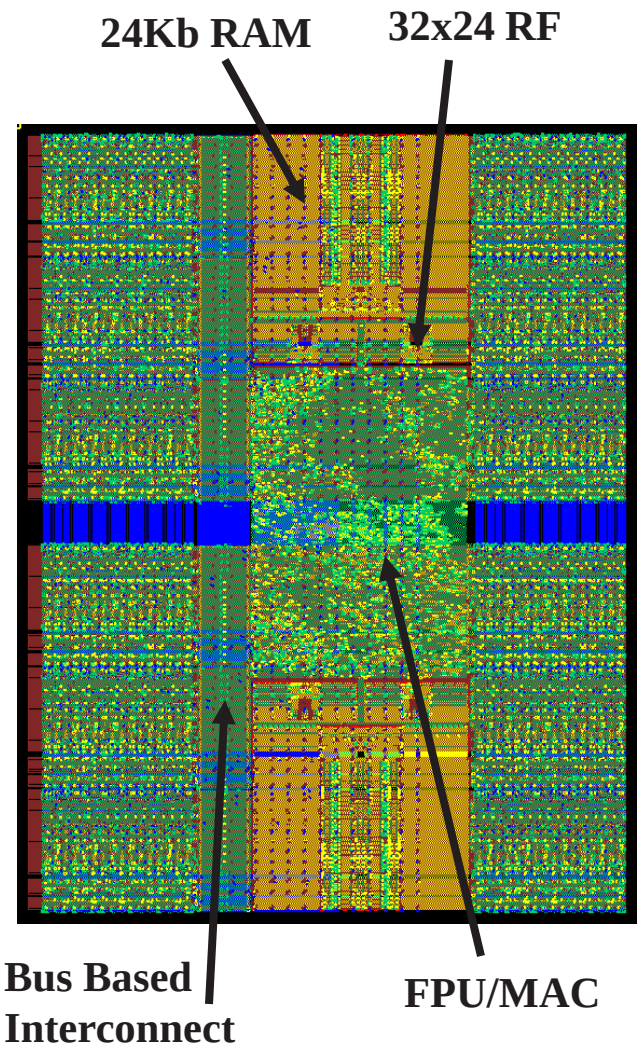
Implemented on CMOS 90GT with 9 layers of metal

Complex logic and routing cells with global and local routes



	Configurable options for Logic and Routing Cell
1	2 independent 4-input Look-Up Tables
2	5 4-input Look-Up Tables with 4 having common inputs
3	2 5-input Look-Up Tables with 4 common inputs
4	1 6 input Look-Up Table
5	Large set of 8 input Functions
6	2 4-to-1 multiplexers with common select lines
7	1 8-to-1 multiplexer
8	1 8-input AND or OR or XOR or other symmetric functions
9	1 4-bit arithmetic adder/subtractor/accumulator with output registers
10	1 8-bit priority encoder
11	1 4-bit loadable shift register
12	Four sequential elements configurable as latch/masterslave and with configurable active high/low clock, load, data enable and synchronous set/clear inputs. An asynchronous reset is also provided.

Signal Processing Engine



Signal Processing Unit Integrates

Computational Element

IEEE Single or Extended Single Floating Point Multiply ADD or,

Fixed Point Multiply Accumulate

(1 36bit, 2 18bit and 4 9bit modes of operation)

Memory Elements –

Two 24Kb Block RAM configurable as memory or FIFO

Four 32x24 Register file configurable as memory, FIFO or Delay Chain

Two-dimensional bus based Interconnect between Processing Units enables predictable 450MHz performance

Silicon Proven

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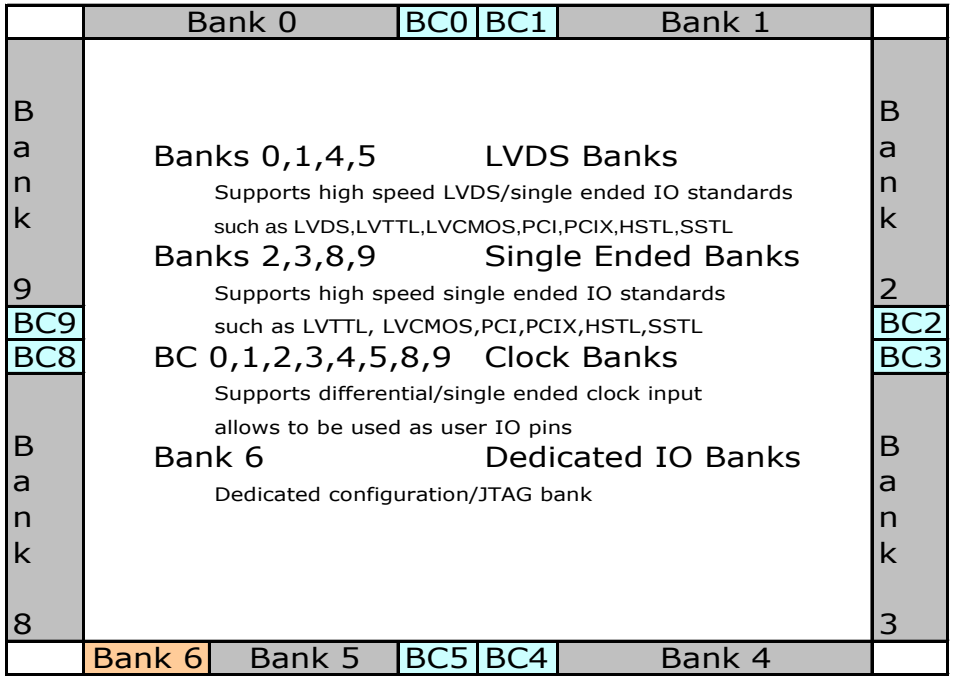
Highly Configurable High Speed IO Banks



Single Ended Banks

- SSTL, HSTL, PCI, PCI-X, LVCMOS, LVTTL Buffers

LVDS Banks

- LVDS up to 1.2 Gbps
- SSTL, HSTL, PCI, PCI-X, LVCMOS, LVTTL at slower speeds

Four 400 MHz DDR2 Interfaces on single chip

- 112 DLLs and dedicated IO clock tree provide configurable strobe clocking for x8,x16,x32,x64
- DDR flops, per bit delay element for each pads

QDR2 SRAM interface using PLLs and IO banks

Support for high speed source synchronous LVDS Bus

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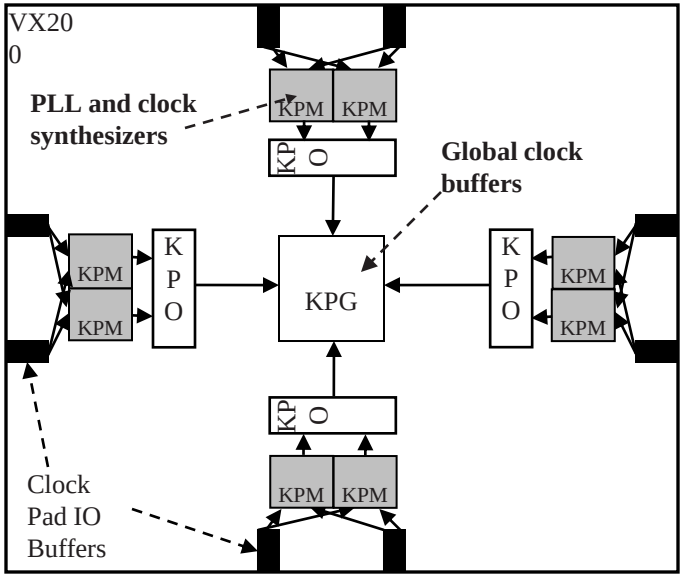
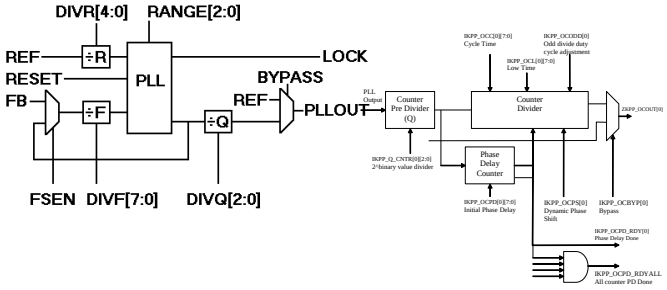
Highly configurable clock subsystem



PLL



Output Synthesizer

- Less than 250 ps of full-chip skew
- 24 high speed, low jitter, wide range, area efficient phase locked loops (PLL) on chip
- 16 output synthesizers provide variable frequency, phase and duty cycle with dynamic phase adjustment
- 16 H-tree global clock network with support for multiple independent clock domains
- Low skew, low jitter hierarchical clock network with flexible local/regional clock network provide up to 24 clock domains
- IO clock and regional clock network allows support for high speed system and memory interfaces

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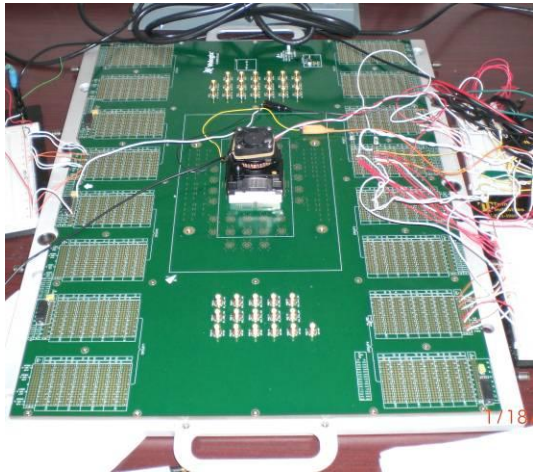
PCBs – Load board and Customer Boards



Load board for use with Agilent 93K Tester
Designed with SMA connectors for clock/IO characterizations
Used in lab to bring up FPGA using JTAG interface (via USB or Ethernet)
Fabric functional at 750MHz

14-layer Customer board designed for Application Accelerator Applications
- Accelerate compute part using Vx200 through PCI-Express Interface

Vx200 provides 180 GFLOP compute density
High memory bandwidth
- Four DDR2 x64 and two QDR2 x36 Interfaces

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